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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,215	07/25/2001	John C. Dute	A-70826/RMA	6832
1678	7590	07/14/2005	EXAMINER	
MARSHALL & MELHORN FOUR SEAGATE, EIGHT FLOOR TOLEDO, OH 43604			PEYTON, TAMMARA R	
			ART UNIT	PAPER NUMBER
			2182	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/916,215

Applicant(s)

DUTE ET AL.

Examiner

Tammara R Peyton

Art Unit

2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 21 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-32 and 39-52 is/are pending in the application.
- 4a) Of the above claim(s) 33-38 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-32 and 39-52 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 17, 20, 22, 25-32, 40, and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Curry et al., (US 5,761,697).

As per claims 1-5, 17, 20, 22, 25-32, 40, and 41, Curry teaches a circuit (2704) for controlling the direction of data traffic, between a first device (computer 2702, Fig. 27) and a second device (2712, 2714, Fig.27), over only a single I/O line (2706, Fig. 27) by utilizing the differences of instantaneous source impedance of a controlling I/O line during data out and data in modes. (Abstract, cols. 49-57)

Curry teaches a circuit (2704) that controls the direction of data traffic between a first and second device via connected bus line that uses the differences of instantaneous source impedance that is changed between a low impedance and a high impedance. It would have been inherent that controlling of input and output data communication is without the presence of any additional signaling protocol that identifies a data input phase or a data output phase.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-16, 18, 19-21, 23, 24, 39-42, 44-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Curry et al., (US 5,761,697).

As per claims 6-9, 18, 19, Curry does not clearly teach wherein a ratio of said high impedance to said low impedance is about or at least 1000:1, 500:1, or 100:1 or between 1000:1 and 10000:1, however, it would have been obvious to one of ordinary skill that the ratio of high/low impedance of Curry's circuit could be modified to implement a host of other ratios, because doing so would ensure the practicality of Curry's circuit when implemented in other systems.

As per claims 39 and 44-47, Curry teaches a peripheral circuit for controlling traffic data signals between a first and second device therefore, it would have been obvious to one of ordinary skill that the adapter would ensure data is routed to the proper destination.

As per claims 10-16, 20, 21, 23, 24, 40, and 41, Curry disclosed the use of a microprocessor in a computer and a connected memory peripheral device and obvious control lines, therefore it would have been obvious that Curry's system could be implemented in other system thereby expanding the flexibility.

As per claims 42 and 48-52, Curry does not teach a data signal and clock signal separation circuit for separation of data-out + clock and data-in at the peripheral device such that it can interface to a standard SPI device or a standard UART at the peripheral device, which is performed such that it can interface to devices which use Pulse Width Modulation to convey analog values. However, separation circuit and the use of Pulse Width Modulation to convey analog values are well known in the art, thereby making their use obvious to one of ordinary skill. (cols. 32-34)

Claims 1-9, 4-16, 39, 42, and 44-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slattery et al., (US 5,361,005).

As per claims 1-5, Slattery teaches a circuit (312) for controlling the direction of data traffic, between a first device (304, Fig. 3) and a second device (308, Fig.3), over only a single I/O line (301, Fig. 3) by utilizing the differences of instantaneous source impedance (low or high) of a controlling I/O line during data out and data in modes. (Abstract, cols. 2-6)

Slattery teaches a peripheral circuit (312) that controls the direction of data traffic between a first and second device via connected bus line that uses the differences of instantaneous source impedance that is changed between a low impedance and a high impedance. It would have been obvious to one of ordinary skill that the controlling of input and output data communication is without the presence of any additional signaling protocol that identifies a data input phase or a data output phase.

As per claims 6-9, Slattery does not clearly teach wherein a ratio of said high impedance to said low impedance is about or at least 1000:1, 500:1, or 100:1 or between 1000:1 and 10000:1, however, it would have been obvious to one of ordinary skill that the ratio of high/low impedance of Kniess' adapter could be modified to implement a host of other ratios, because doing so would ensure the practicality of Kniess' adapter when implemented in other systems.

As per claims 39 and 44-47, Slattery teaches a peripheral circuit for controlling traffic data signals between a first and second device therefore, it would have been obvious to one of ordinary skill that the adapter would ensure data is routed to the proper destination.

As per claims 14-16, Slattery disclosed in a prior art system the use of a microprocessor and a memory peripheral device and obvious control lines, therefore it

would have been obvious that Slattery's system could be implemented in other system thereby expanding the flexibility.

As per claims 42 and 48-52, Slattery does not teach a data signal and clock signal separation circuit for separation of data-out + clock and data-in at the peripheral device such that it can interface to a standard SPI device or a standard UART at the peripheral device, which is performed such that it can interface to devices which use Pulse Width Modulation to convey analog values. However, separation circuit and the use of Pulse Width Modulation to convey analog values are well known in the art, thereby making their use obvious to one of ordinary skill.

Claims 1-32 and 39-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Little et al., (US 6,412,072).

As per claims 1-5, 10-17, 20-32, 40, and 41 Little teaches a circuit for controlling the direction of data traffic, between a first device (Fig. 2) and a second device (Fig.2), over only a single I/O line by utilizing the differences of instantaneous source impedance (low or high) of a controlling I/O line during data out and data in modes. (Abstract, cols. 2-39)

Little teaches a circuit that controls the direction of data traffic between a first and second device via connected bus line that uses the differences of instantaneous source impedance that is changed between a low impedance and a high impedance. It would

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have been obvious to one of ordinary skill that the controlling of input and output data communication is without the presence of any additional signaling protocol that identifies a data input phase or a data output phase.

As per claims 6-9, 18, 19, Little does not clearly teach wherein a ratio of said high impedance to said low impedance is about or at least 1000:1, 500:1, or 100:1 or between 1000:1 and 10000:1, however, it would have been obvious to one of ordinary skill that the ratio of high/low impedance of Little circuit could be modified to implement a host of other ratios, because doing so would ensure the practicality of Little's circuit when implemented in other systems.

As per claims 39 and 44-47, Little teaches a peripheral circuit for controlling traffic data signals between a first and second device therefore, it would have been obvious to one of ordinary skill that the adapter would ensure data is routed to the proper destination.

As per claims 42, 48, and 49-52, Little does not teach a data signal and clock signal separation circuit for separation of data-out + clock and data-in at the peripheral device such that it can interface to a standard SPI device or a standard UART at the peripheral device, which is performed such that it can interface to devices which use Pulse Width Modulation to convey analog values. However, separation circuit and the



use of Pulse Width Modulation to convey analog values are well known in the art, thereby making their use obvious to one of ordinary skill.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammara Peyton whose telephone number is (571) 272-4157. The examiner can normally be reached between 6:30 - 4:00 from Monday to Thursday, (I am off every first Friday), and 6:30-3:00 every second Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici, can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3718.

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Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Mailed responses to this action should be sent to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231.

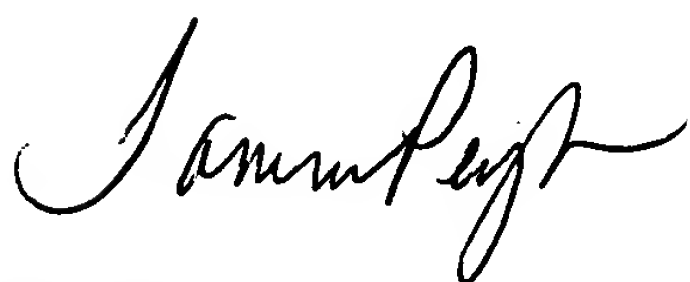
Faxes for Official/formal (After Final) communications or for informal or draft communications (please label "PROPOSED" or "DRAFT") sent to:

(703) 872-9306

Hand-delivered responses should be brought to:

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Crystal Plaza Two, Lobby Room 1B03, Arlington, VA, 22202Crystal Park II, 2121.



Tammara Peyton

July 9, 2005